**IN THE CLAIMS:**

Please cancel claims 5-6 without prejudice, and amend the claims as follows:

1. (Currently Amended) A dynamic memory cell, comprising:

a storage capacitor;

a first selection transistor; and

a second selection transistor; wherein depending on a selection signal, a first electrode of the storage capacitor is connected to a first bit line via the first selection transistor and a second electrode of the storage capacitor is connected to a second bit line via the second selection transistor;

wherein the first and second selection transistors are vertically disposed on opposite sides of the storage capacitor, respectively;

wherein the storage capacitor comprises an inner region defining the first electrode, an outer region defining the second electrode and an insulation layer disposed between the regions to electrically isolate the regions from one another;

wherein the first selection transistor is connected to the inner region and the second selection transistor is connected to the outer region; and

wherein, when the selection transistors is activated, a charge of the inner region is applied to the first bit line and a charge of the outer region is applied to the second bit line.

2. (Original) The cell of claim 1, wherein the storage capacitor, the first selection transistor and the second selection transistor are disposed between the bit lines at a location where the bit lines are parallel to one another.

3. (Original) The cell of claim 1, wherein the storage capacitor, the first selection transistor and the second selection transistor are disposed on a substrate and wherein the first and second selection transistors are in a vertically stacked arrangement relative to the storage capacitor.

4. (Original) The cell of claim 1, wherein, in the event of the selection transistors being activated, a charge of the first electrode is applied to the first bit line and a charge of the second electrode is applied to the second bit line.

5. (Canceled) The cell of claim 1, wherein the storage capacitor comprises an inner region defining the first electrode, an outer region defining the second electrode and an insulation layer disposed between the regions to electrically isolate the regions from one another; wherein the first selection transistor is connected to the inner region and the second selection transistor is connected to the outer region, so that, in the event of the selection transistors being activated, a charge of the inner region is applied to the first bit line and a charge of the outer region is applied to the second bit line.

6. (Canceled) The cell of claim 5, wherein the first and second selection transistors are vertically disposed on either side of the storage capacitor.

7. (Currently Amended) A DRAM circuit, comprising:

a) a pair of bit lines comprising a first bit line and a second bit line;

b) a plurality of dynamic memory cells coupled between the pair of bit lines, each dynamic memory cell comprising:

a storage capacitor for storing a charge representative of a bit value;

a first selection transistor coupled to a first electrode of the storage capacitor; and

a second selection transistor coupled to a second electrode of the storage capacitor; wherein the first and second selection transistors are vertically disposed on ~~either side~~ opposite sides of the storage capacitor, respectively, and wherein, depending on a selection signal, the first electrode of the storage capacitor is connected to the first bit line via the first selection transistor and the second electrode of the storage capacitor is connected to the second bit line via the second selection transistor, ~~so that, in the event of~~ wherein, when the selection transistors ~~being~~ are activated, a charge of the first electrode is applied

to the first bit line and a charge of the second electrode is applied to the second bit line; and

c) a word line coupled to the selection transistors and configured to drive the selection transistors.

8. (Original) The DRAM circuit of claim 7, further comprising a sense amplifier coupled to the pair of bit lines.

9. (Original) The DRAM circuit of claim 7, wherein the storage capacitor, the first selection transistor and the second selection transistor of each dynamic memory cell are disposed between the bit lines at a location where the bit lines are parallel to one another.

10. (Original) The DRAM circuit of claim 7, wherein the bit lines cross over each other at least once along their respective lengths.

11. (Withdrawn) A DRAM circuit disposed on a substrate, comprising:

a) a pair of bit lines comprising a first bit line and a second bit line;

b) a memory cell, comprising:

a trench capacitor, comprising an inner region defining a first electrode, an outer region defining a second electrode and an insulation layer electrically isolating the inner and outer regions from one another;

a first selection transistor coupled to the inner region of the trench capacitor; and

a second selection transistor coupled to the outer region of the trench capacitor wherein the first and second selection transistors are vertically disposed on either side of the trench capacitor; wherein, in the event of the selection transistors being activated, a charge of the inner region is applied to the first bit line and a charge of the outer region is applied to the second bit line;

c) a conductive drive region disposed between the selection transistors and to which a drive signal is applied for activation of the selection transistors;

d) an insulator disposed on the drive region; and

e) a word line coupled to the drive region and configured to allow selection of the selection transistors.

12. (Withdrawn) The DRAM circuit of claim 11, wherein the drive region is disposed over the trench capacitor.

13. (Withdrawn) The DRAM circuit of claim 11, further comprising a sense amplifier coupled to the pair of bit lines.

14. (Withdrawn) The DRAM circuit of claim 11, wherein the drive region is configured to serve as a gate region for the first and the second selection transistors.

15. (Withdrawn) The DRAM circuit of claim 11, wherein a first drain/source region of the first selection transistor contacts the inner region of the trench capacitor and a second drain/source region of the second selection transistor contacts the outer region of the trench capacitor.

16. (Withdrawn) The DRAM circuit of claim 15, wherein the drive region is configured to serve as a gate region for the first and the second selection transistors.

Please add the following new claims:

17. (New) The cell of claim 1, wherein the first selection transistor comprises:
a first source/drain region disposed at a surface of a substrate;
a first channel region disposed below the first source/drain region; and
a second source/drain region disposed below the channel region.

18. (New) The cell of claim 17, wherein the first and second source/drain regions comprise $n^+$-doped regions of in the substrate.

19. (New) The cell of claim 18, wherein the second selection transistor comprises:

a third source/drain region disposed at the surface of the substrate;

a second channel region disposed below the third source/drain region; and

a fourth source/drain region disposed below the second channel region, wherein the third and fourth source/drain regions comprise $n^+$-doped regions of in the substrate.

20. (New) The cell of claim 19, wherein the first source/drain region is electrically connected to the first bit line, wherein the second source/drain region is electrically connected to the first electrode of the storage capacitor, wherein the third source/drain region is electrically connected to the second bit line, and wherein the fourth source/drain region is electrically connected to the second electrode of the storage capacitor.

21. (New) The DRAM circuit of claim 7, wherein the each selection transistor comprises:

a first source/drain region disposed at a surface of a substrate;

a channel region disposed below the first source/drain region; and

a second source/drain region disposed below the channel region, wherein the third and fourth source/drain regions comprise $n^+$-doped regions of in the substrate.

22. (New) The DRAM circuit of claim 7, further comprising:

one or more pairs of bit lines; and

a further plurality of dynamic memory cells coupled between each pair of bit lines, wherein, for each adjacent pairs of bit lines, one pair of bit lines includes bit lines that cross over each other between adjacent dynamic memory cells connected to the respective pair of bit lines.